ABSTRACT OF THE DISCLOSURE

The present invention is broadly directed to a memory system comprising a a host integrated circuit component, at least two data memories, at least one parity memory for storing parity information corresponding to data stored in a corresponding address space of the data memories, and at least two controller integrated circuits. Each controller integrated circuit (IC) comprises memory control logic configurable to control communications between the controller IC and data memories directly connected to the controller IC, parity logic configurable to compute parity information for data communicated to or from the data memories, logic configurable to communicate the parity information to or from a companion IC, and logic configurable to communicated data to or from a companion IC.